**THAT WHICH IS CLAIMED IS:**

add a1

1. DRAM memory integration method, where each memory cell, defined by a bit line (2) and a word line (1), is composed of a storage capacitance and an access transistor, said method being characterized in that it comprises the following steps consisting of:

a) depositing a barrier layer (10) followed by a silicon oxide layer (TEOS);

b) photoetching the silicon oxide (TEOS) so as to define cylinders (11) wherein the capacitances are to be formed;

c) depositing a first polysilicon layer to form the lower electrode (elec 1) of the capacitances;

d) carrying out mechano-chemical polishing to remove the polysilicon from said first layer between the capacitances;

e) removing the silicon oxide layer (TEOS) so as to create a difference in topography between each lower electrode (elec 1) and the silicon oxide layer (TEOS);

f) depositing a dielectric layer;

g) depositing a second doped polysilicon layer so as to form a continuous upper electrode plate (elec 2), the different in topography being only retained in a zone (A) where it is necessary to open said upper electrode plate (elec 2) to insert the bit line contact;

h) depositing a third non-doped polysilicon layer (poly3);

i) carrying out a very significantly inclined implantation of dopants of the third non-doped polysilicon layer (poly3) so as only to implant the upper part of said layer located in the zone (A) showing the difference in topography;

j) carrying out a selective etching to only remove the part of the non-doped polysilicon layer

(poly3) located in the lower part of said zone (A);

k) carrying out etching to remove the entire remainder of the third polysilicon layer (poly3) and the part of the upper electrode layer (elec 2) located in said lower part, the removal of the upper electrode layer (elec 2) being self-aligned on the lower electrode (elec 1).

2. Method according to claim 1 characterized in that step i is preceded by an additional step in the case of an embedded DRAM memory consisting of using a mask so that the part of the non-doped polysilicon layer (poly3) covering the logical circuits is not implanted.

3. Method according to claim 1 or 2 characterized in that the lower electrode (elec 1) is deposited in the form of hemispherical polysilicon grains.

4. Method according to claim 1 or 2 characterized in that step e is carried out by chemical etching, the depth removed being determined by the etching time.

5. Method according to claim 1 or 2 characterized in that the dielectric deposited in step f is formed from two layers, one oxide layer and one nitride layer.

6. Method according to claim 1 or 2 characterized in that the implantation carried out in step i is performed with $BF_2$ dopants.

7. Method according to claim 1 or 2 characterized in that wet solutions such as KOH or $NH_4OH$ are used for the selective removal in step j.

8. Method according to claim 1 or 2 characterized in that the etching carried out in step k is plasma ion etching.

9. Method according to claim 8, characterized in that said etching is carried out isotropically.

10. Method according to claim 8, characterized in that said etching is carried out anisotropically.